REMARKS/ARGUMENTS

After entry of this amendment, claims 1-12 and 46-53 will remain pending in this application. Claim 1 has been amended. Support for the amended claim can be found in the specification. No new matter has been added.

Claims 1-4, 7-10, 46-51, and 53 stand rejected under 35 U.S.C.§ 103(a) as being unpatentable over Winegarden et al., United States patent number 6,467,009, in view of Sugita, United States patent number 5,276,842. Claims 5, 6, 11, 12, and 52 stand rejected under 35 U.S.C.§ 103(a) as being unpatentable over Winegarden in view of Sugita, and further in view of Phelan, United States patent number 6,499,089. Reconsideration of these rejections and allowance of the pending claims is respectfully requested.

Drawings

Figure 7 of the drawings has been objected to. Specifically, the pending office action states that there are unreadable context marks that were printed with graphite. Neither the applicants nor their representative recall writing on this figure. It is surmised that comments pertaining to text size may have been written on this figure by a someone at the USPTO. To this end, a replacement sheet where the text is enlarged is included with this amendment. No substantive changes were made to this figure.

Claim 1

Claim 1 stands rejected under 35 U.S.C.§ 103(a) as being unpatentable over Winegarden in light of Sugita. But this combination of references does not teach each and every limitation of this claim. For example, claim 1, as amended, recites:

> wherein when the second port is accessing a subset of the first plurality of memory cells, the arbiter <u>prevents</u> the first port from accessing the <u>first</u> plurality of memory cells but <u>allows</u> the first port to access the <u>second</u> plurality of memory cells, and when the second port is accessing a subset of the second plurality of memory cells, the arbiter <u>allows</u> the first port to access the <u>first and second</u> pluralities of memory cells. (applicants' claim 1, emphasis added.)

The cited references do not provide this feature either alone or in combination.

The pending office action cites Sugita, Figure 10, column 7, line 34 through column 8, line 49, and column 20, lines 16-27 as providing this. (See pending office action, page 5.) However, the first of these passages only states that an arbitration circuit is used and that it determines whether an access contention exits between its two ports. (See Sugita, column 7, lines 39 and 40.) The second passage states that arbitration between read and write access must be done in the disclosed system. (See Sugita, column 20, lines 17 and 18.) From this, Sugita discloses an arbiter wherein when a first port is accessing a first subset of memory cells, the second port can access any memory cells that are not in the first subset. In Sugita, only an access that would result in a direct contention is prevented. This does not anticipate the arbiter preventing access to a first plurality of memory cells but allowing access to a second plurality of memory cells by a first port when a subset of the first plurality of memory cells is being accessed by a second port, and allowing access to either the first or second pluralities of memory cells by the first port when a subset of the second plurality of memory cells is being accessed by the second port, as required by the claim.

For at least these reasons, claim 1 should be allowed.

Claim 7

Claim 7 stands rejected under 35 U.S.C.§ 103(a) as being unpatentable over Winegarden in light of Sugita. But this combination of references do not show or suggest each and every element of this claim. For example, claim 7 recites:

> wherein when the second port is accessing a subset of the first plurality
> of memory cells, the arbiter prevents the first port from accessing the first plurality of
> memory cells, and when the second port is accessing the subset of the first plurality of
> memory cells, the arbiter allows the first port to access the second plurality of memory
> cells. (applicants' claim 7, emphasis added.)

The cited references do not provide this feature.

The pending office action cites Sugita, Figure 10, column 7, line 34 through column 8, line 49, and column 20, lines 16-27 as providing this. (See pending office action, page 5.) However, as mentioned above, the first of these passages only states that an arbitration circuit is used and that it determines whether an access contention exits between its two ports.

Application number 09/881,226   <u>PATENT</u>
Amendment dated January 26, 2006
Reply to office action mailed July 26, 2005

(See Sugita, column 7, lines 39 and 40.) The second passage states that arbitration between read and write access must be done in the disclosed system. (See Sugita, column 20, lines 17 and 18.) From this, Sugita discloses an arbiter wherein when a first port is accessing a first subset of memory cells, the second port can access any memory cells that are not in the first subset. In Sugita, only an access that would result in a direct contention is prevented. This does not anticipate the arbiter <u>preventing access to a first plurality of memory cells</u> and <u>allowing access to a second plurality of memory cells by a first port</u> when a subset of the first plurality of memory cells is being accessed by a second port, as required by the claim.

For at least these reasons, claim 7 should be allowed.

<u>Claim 47</u>

Claim 47 stands rejected under 35 U.S.C.§ 103(a) as being unpatentable over Winegarden in light of Sugita. But this combination of references do not show or suggest each and every element of this claim. For example, claim 47 recites:

> wherein when the first port is accessing a subset of the first plurality of memory cells, <u>the arbiter prevents the second port from accessing the first plurality of memory cells</u> and <u>allows the second port to access the second plurality of memory cells,</u> and

> wherein <u>the first plurality of memory cells consists of a number of memory cells and the number is configurable.</u> (applicant's claim 47, emphasis added.)

The cited references do not provide this feature.

It is not clear from the pending office action what the reasoning for the rejection of this claim is. But as discussed above, Sugita discloses an arbiter wherein when a first port is accessing a first subset of memory cells, the second port can access any memory cells that are not in the first subset. In Sugita, only an access that would result in a direct contention is prevented. As described above, this does not anticipate the arbiter <u>preventing access to a first plurality of memory cells</u> and <u>allowing access to a second plurality of memory cells by a second port</u> when a subset of the first plurality of memory cells is being accessed by a first port, as required by the claim. Further, it does not anticipate the <u>first plurality of memory cells</u>

consisting of a number of memory cells where the first number is configurable, which is also required by the claim.

For at least these reasons claim 47 should be allowed.

Other claims

The other claims depend on these claims, and should be allowed for at least the same reasons and for the additional limitations they recite.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this application are in condition for allowance. The issuance of a formal notice of allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

J. Matthew Zigmant
Reg. No. 44,005

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 415-576-0200
Fax: 415-576-0300
Attachments
JMZ:jmz
60625776 v1